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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,032	10/03/2005	Andreas Lindemann	1477.021	6968

23405 7590 03/15/2007

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EXAMINER	
BAUMAN, SCOTT E	
ART UNIT	PAPER NUMBER
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,032	LINDEMANN, ANDREAS	
	Examiner	Art Unit	
	Scott E. Bauman	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03 October 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 03 October 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 1, element 18. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-11, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Noda et al, United States Patent 5, 767,573.

En re Claim 1, Noda et al '573 discloses a substrate (Fig 7, item 305) of a ceramic insulation material (Col 12, lines 25-33) with islands (Fig 7, item 306) comprising a thermally and electrically conductive material (Col 12, lines 34-36, examiner's note: it is well known in the art that copper is a thermally and electrically conductive material), at least two power semiconductor chips (Fig 7, items 301a and 301b) arranged on the islands (Fig 7, item 306), electrical connections (Fig 6, Items W1, W2, W3, and W4) from the chips (Fig 7, items 301a and 301b) to connecting elements (Fig 7, items 103a and 103b), wherein at least two connecting elements (Fig 7, items 103a and 103b) are electrically connected (Fig 6, Items W1, W2, W3, and W4) to the islands (Fig 7, item 306), wherein an enclosure (Fig 6, item MR) of pressed plastic material (Col 13, line 2) is provided which fully surrounds the power semiconductor chips (Fig 6, items 301a and 301b) and at least partially surrounds the substrate (Fig 6, item 305), wherein the connecting elements (Fig 6, items 103a and 103b) are designed as flat conductor connections projecting from the enclosure (Fig 6), and the substrate

(Fig 6, item 305) exhibits a metal coating (Fig 6, item 307) on a side opposite (Fig 6) the islands (Fig 6, item 306).

FIG. 6

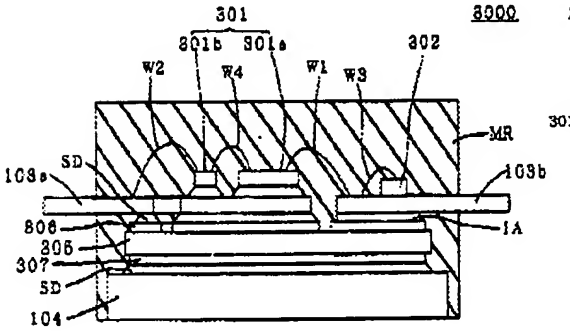
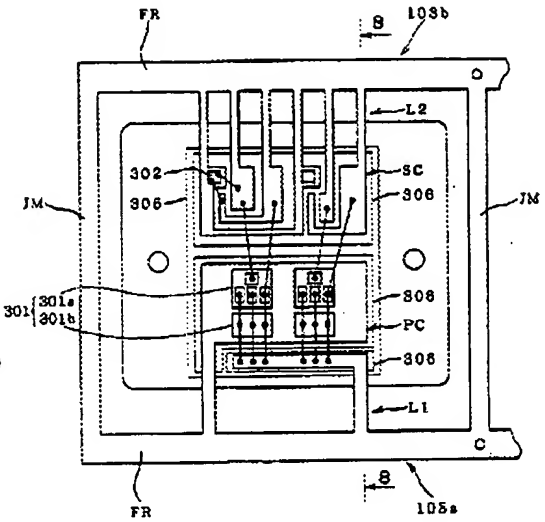


FIG. 7

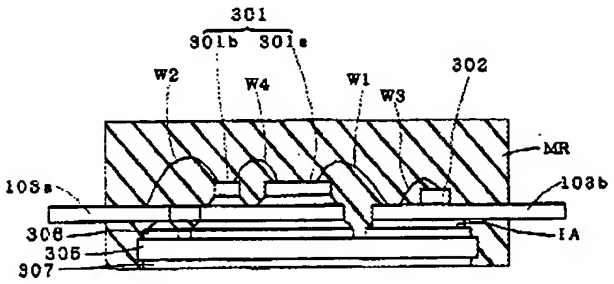


En re Claim 2, Noda et al '573 discloses wherein the islands (Fig 7, item 306) include separate partial surfaces (Col 13, lines 7-8) of a metal layer (Col 12, lines 34-36).

En re Claim 3, Noda et al '573 discloses wherein the substrate is a ceramic substrate which contains, aluminium oxide (Col 12, lines 27-28) or aluminium nitride ceramic material (Col 12, lines 30-31).

En re Claim 4, Noda et al '573 discloses wherein the metal coating (Fig 8, item 307) of the substrate (Fig 8, item 305) is at least partially exposed (Col 13, line 57-62) on the side opposite the islands (Fig 8, item 306).

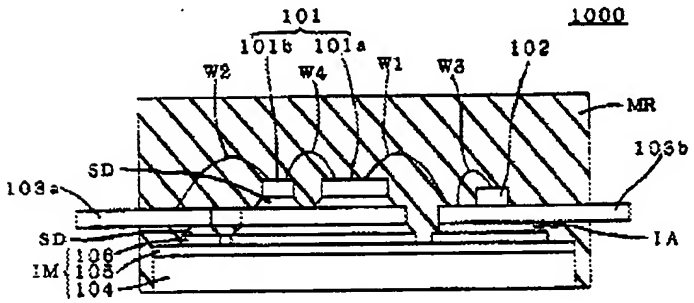
FIG. 8



En re Claim 5, Noda et al '573 discloses wherein the substrate is a direct-copper-bond (Col 12, line 25) or direct-aluminium-bond substrate.

En re Claim 6, Noda et al '573 discloses wherein the electrical connections comprise soldered connections (Fig 1, item SD).

FIG. 1



En re Claim 7, Noda et al '573 discloses wherein the electrical connections (Fig 7, items W1, W2, W3, and W4) comprise wire connections (Col 12, lines 54-61) and/or connections via the islands.

En re Claim 8, Noda et al '573 discloses wherein the connecting elements (Fig 7, items 103a and 103b) are located on two different sides of the enclosure (Fig 7).

En re Claim 9, Noda et al '573 discloses wherein the connecting elements (Fig 7, item 103a) are arranged and connected to the chips (Fig 7, item 301) so that connecting

elements conducting (Fig 7, item L1) a main current are arranged adjacent to each other (Fig 7, item 301).

En re Claim 10, Noda et al '573 discloses wherein the connecting elements (Fig 7, items 103a and 103b) are arranged and connected to the chips (Fig 7, item 301) so that two connecting elements (Fig 7, item L2), which are provided with potentials which have a high mutual potential difference, are arranged further from each other than two connecting elements with potentials which have a low mutual potential difference (Fig 7, items L1).

En re Claim 11, Noda et al '573 discloses wherein the chips (Fig 1, item 101) are secured to a metal island (Fig 1, item 106) by means of soldered connections (Fig 1, item SD).

En re Claim 13, Noda et al '573 discloses wherein the chips comprise MOSFET, diode (Fig 7, item 301b), IGBT (Fig 7, item 301a) and/or thyristor chips.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al, United States Patent 5,767,573 as applied to claim 1 above, and further in view of Ito et al, United States Patent 5,198,964.

Noda et al '573 does not disclose wherein at least one shoulder is formed on a bottom of the enclosure for inserting a flat insulator.

Ito et al '964 discloses wherein at least one shoulder is formed on a bottom of the enclosure for inserting a flat insulator.

It would have been obvious to one of ordinary skill in the art at the time the invention was made, to have modified Noda et al '573 Semiconductor Device with Ito et al '964 Packaged Semiconductor Device And Electronic Device Module Including The Same to provide a technique to which can avoid any short-circuiting caused by improper soldering or electrically conductive bonding material.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noda et al, United States Patent 5,767,573 as applied to claim 1 above, and further in view of Triantafyllou et al, United States Patent 6,841,869.

Noda et al '573 does not discloses wherein the chips, when interacting, form an individual switch, a chopper, a bridge branch, an H-bridge or a three phase bridge or a combination of these elements.

Triantafyllou et al '869 discloses wherein the chips, when interacting, form an individual switch (Col 2, lines 4-6), a chopper, a bridge branch, an H-bridge (Col 2, lines 4-6) or a three phase bridge or a combination of these elements.

It would have been obvious to one of ordinary skill in the art at the time the invention was made, to have modified Noda et al '573 Semiconductor Device with Triantafyllou et al '869 Electronic Package Assembly because an assembly is provided which has improved integration and good thermal management (Col 2, lines 15-17).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fukunaga, United States Patent 5,077,595 discloses bridge power switching devices. Eytcheson et al, United States Patent 5,523,620 discloses dual switch power module, Iversen et al, United States Patent 6,160,326 discloses a three phase power output driver. Takahashi, United States Patent 5,825,082 discloses an H Bridge circuit. Hable, United States Patent Application Publication 2003/0112605 discloses a power module with a three phase output.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott E. Bauman whose telephone number is 571-270-1443. The examiner can normally be reached on M-TH 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Scott Bauman
Examiner.

EUGENE LEE
PRIMARY EXAMINER